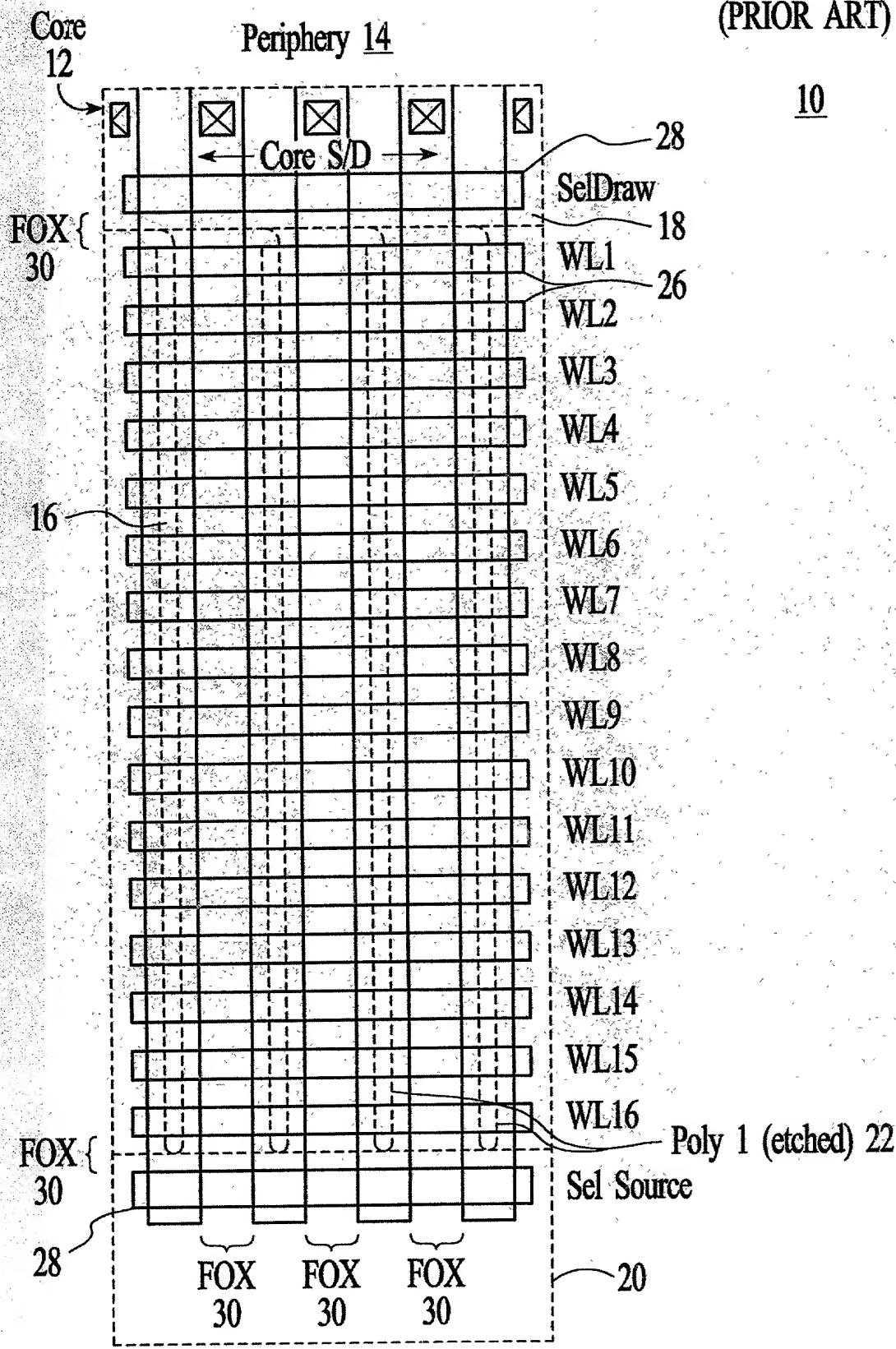


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**FIG. 1**  
**(PRIOR ART)**



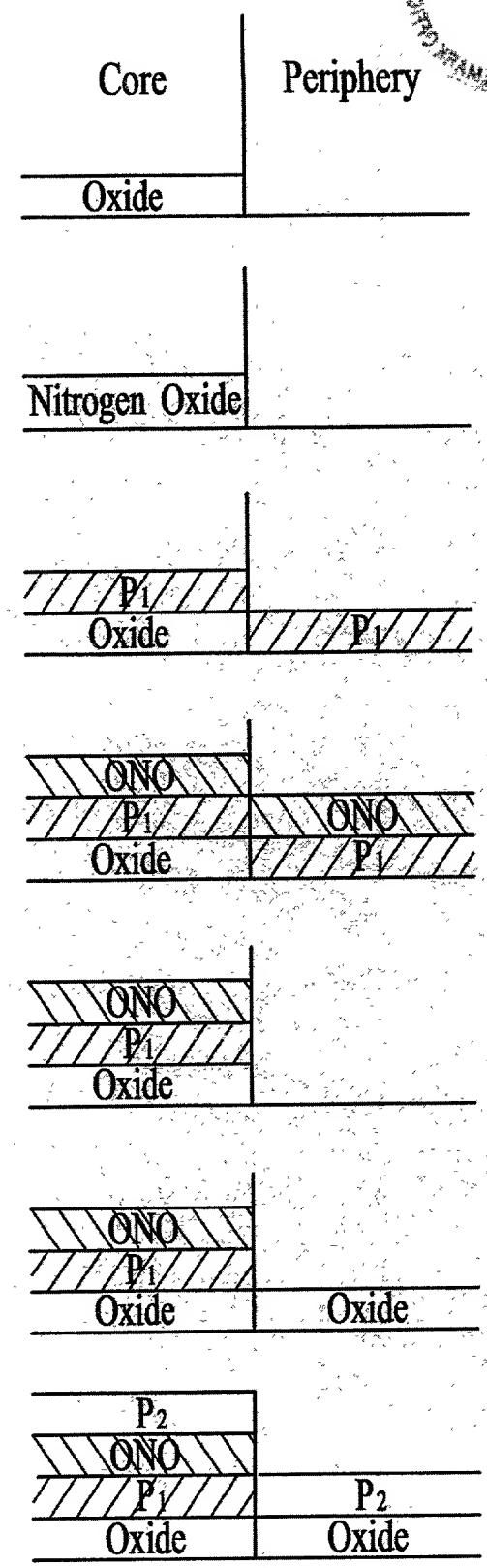
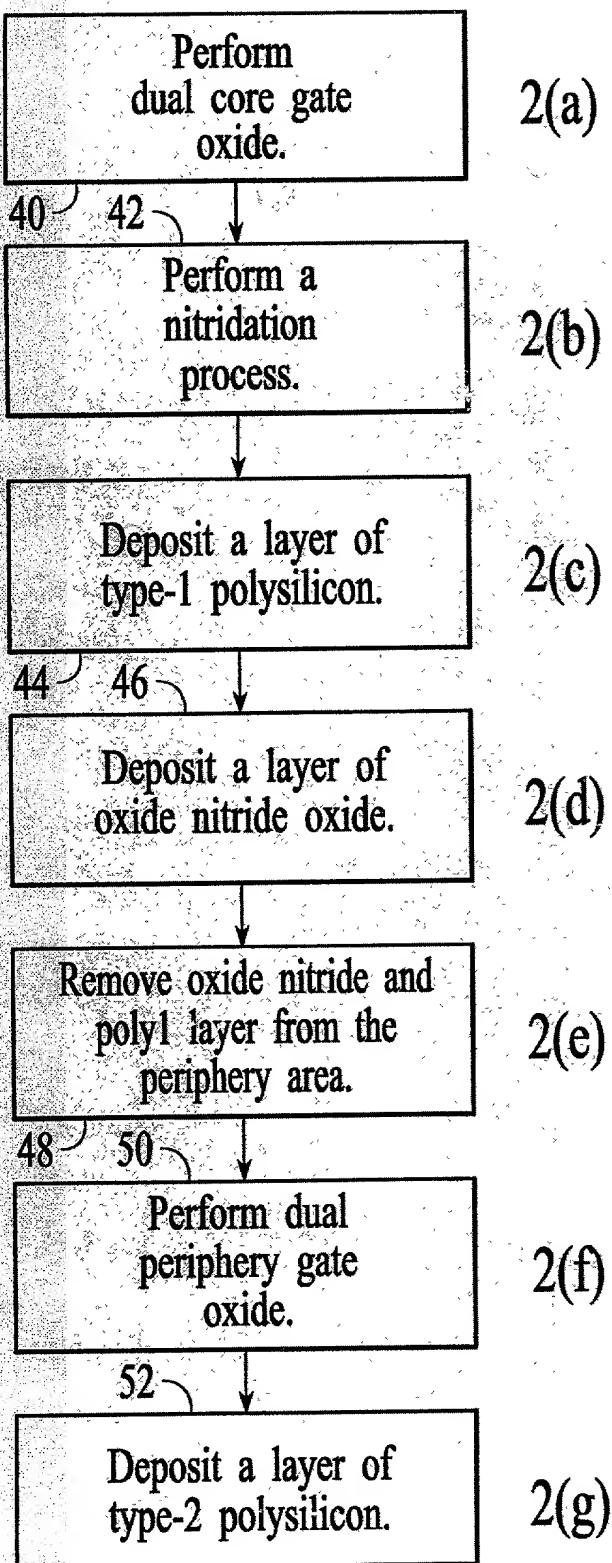
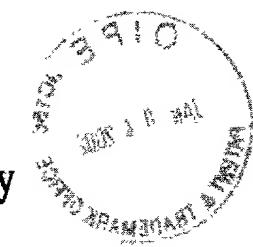


FIG. 2 (PRIOR ART)



Provide a portion of the dual periphery gate oxide.

200 202

Provide a dual core gate oxide and complete the dual periphery gate oxide.

Provide a nitridation process.

204 206

Deposit a layer of type-1 polysilicon.

Deposit a layer of oxide nitride oxide.

208 210

Remove oxide nitride and a portion of the poly1 layer from the periphery area.

Deposit a layer of type-2 polysilicon.

212

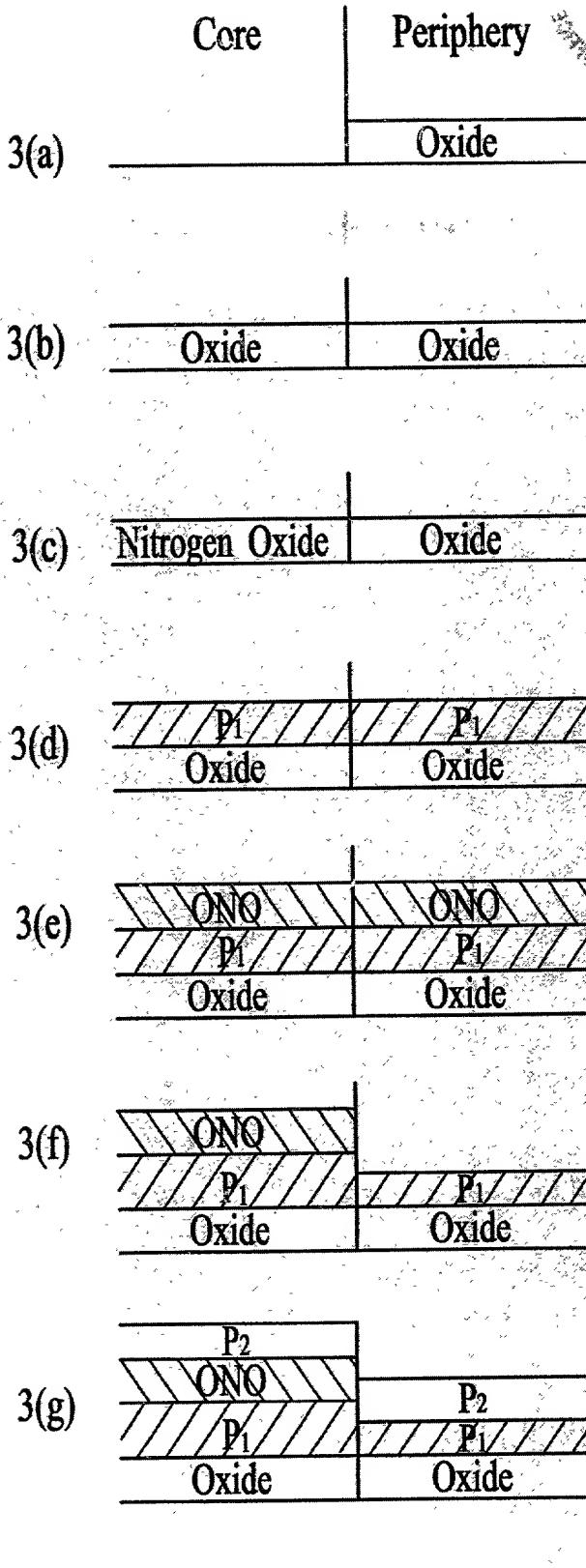


FIG. 3

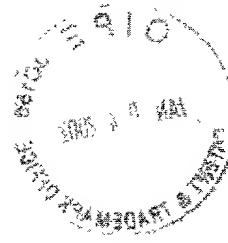
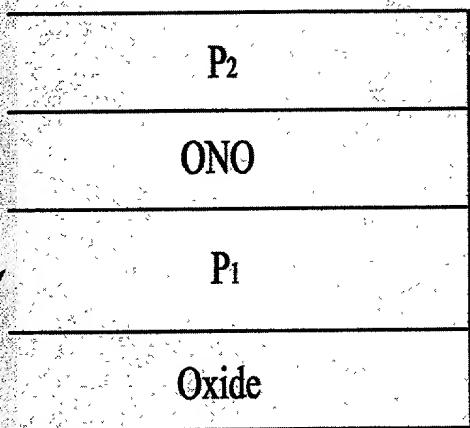
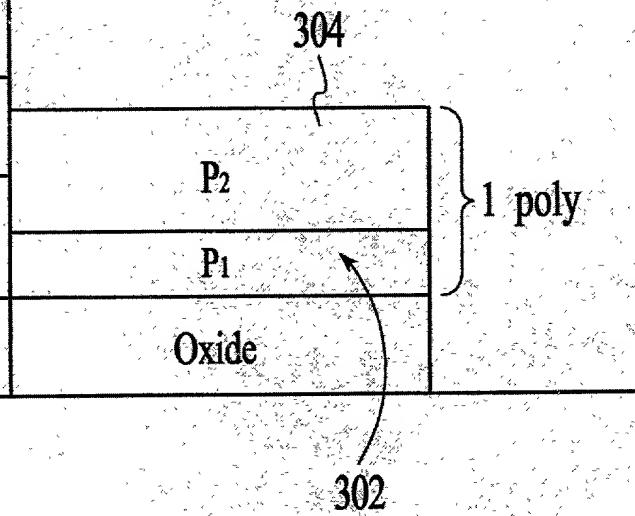
CorePeriphery

FIG. 4